*Problem statement-four types of fast adders implementing in Verilog using structure model.*

1. **Carry look ahead adder:**

Carry Look Ahead (CLA) design is based on the principle of

looking at lower adder bits of argument and addend if higher orders

carry generated. This adder reduces the carry delay by reducing

the number of gates through which a carry signal must propagate

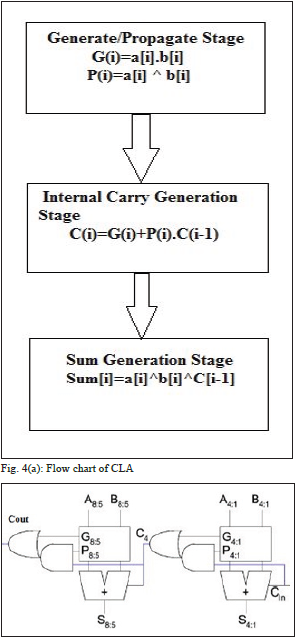
[2]. In the generation and propagation stage,

the generation values, propagation values are computed. Internal

carry generation is calculated in second stage.

And in final stage, the sum is calculated. .

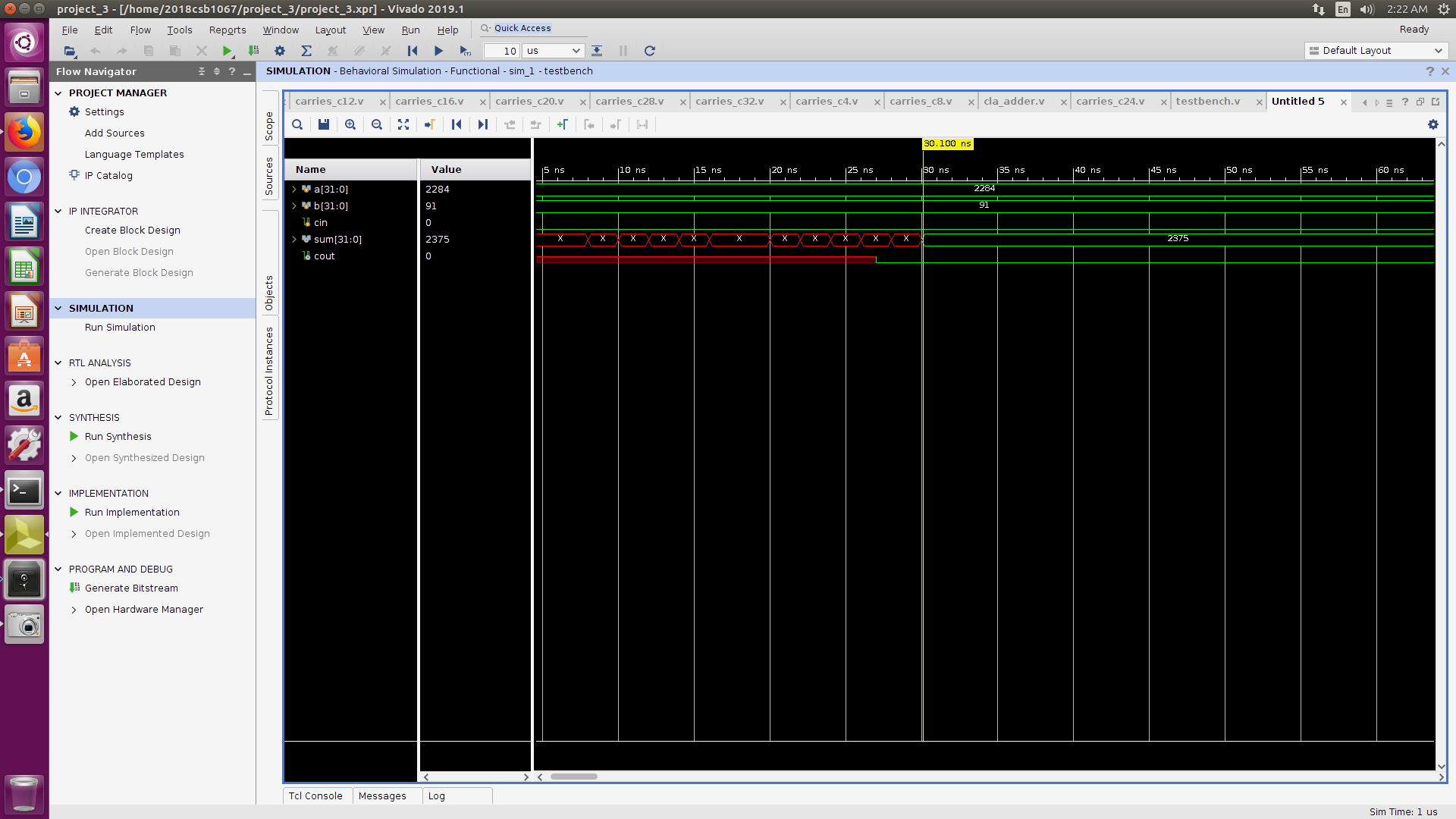
DIAGRAM:



**Delay:**

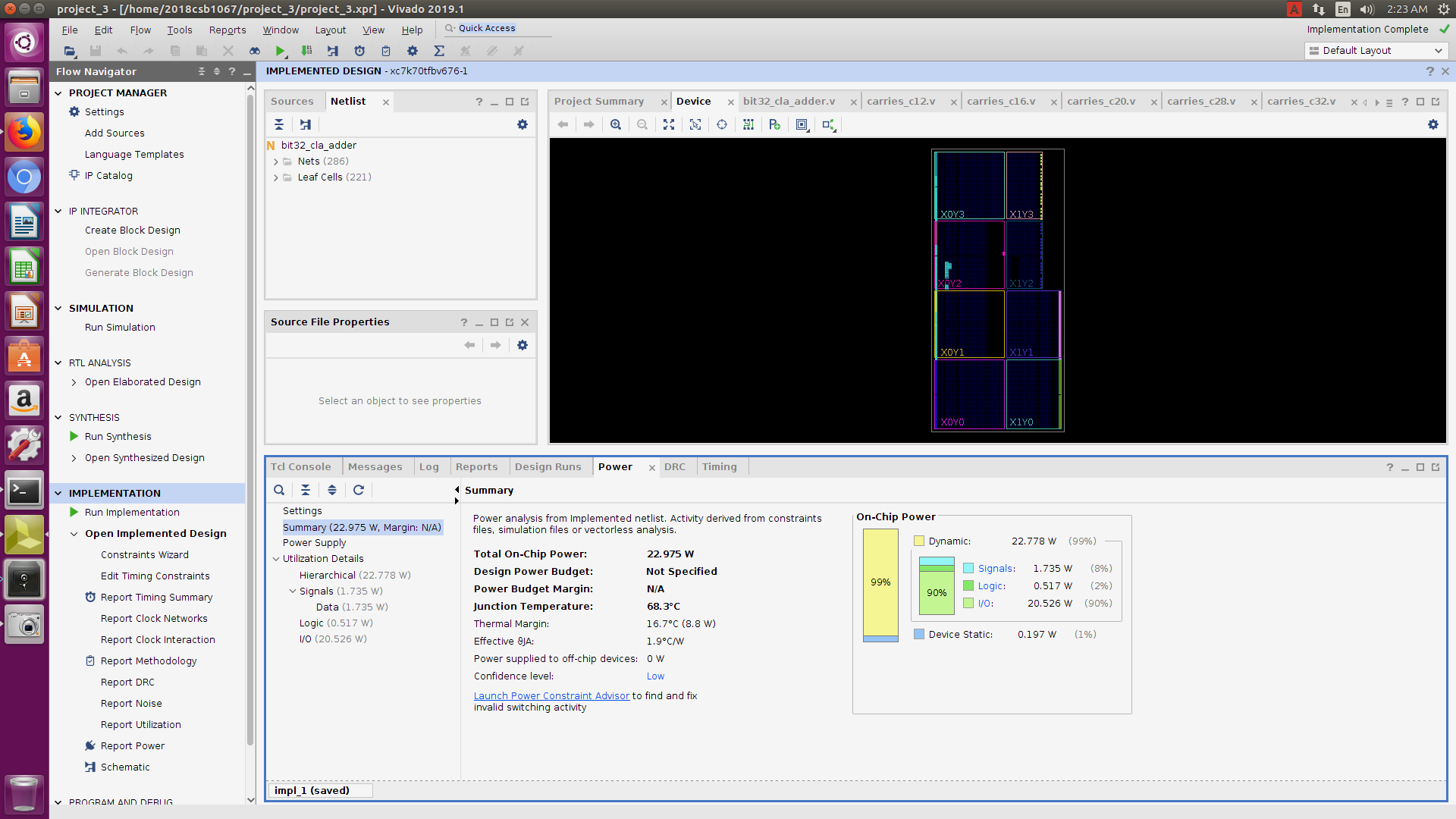
The delay and output graph of CLA is attached below for a given set of input.

CLA is the most delay efficient adder as would be visible by figure.



POWER ANALYSIS:

The power consumed of the given adder is as estimated as follows:



**CARRY SELECT ADDER:**

Carry Select Adder (CSlA) architecture consists of independent

generation of sum and carry i.e., Cin=1 and Cin=0 are executed

parallelly . Depending upon Cin, the external multiplexers

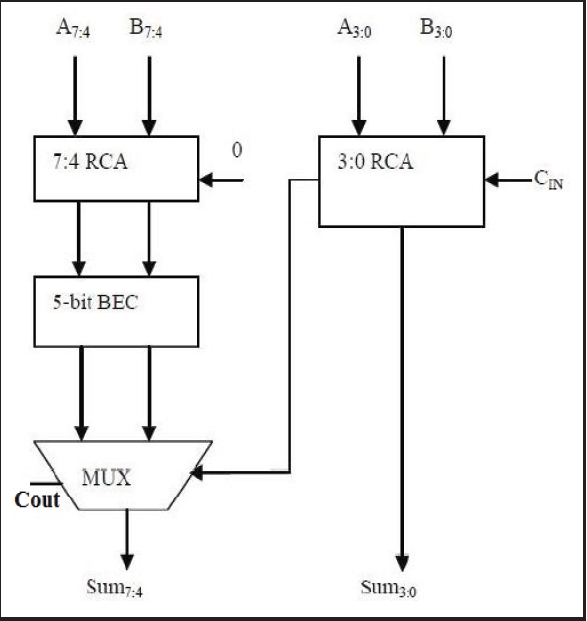
select the carry to be propagated to next stage. Further, based

on the carry input, the sum will be selected. Hence, the delay is

reduced.

However, the structure is increased due to the complexity of

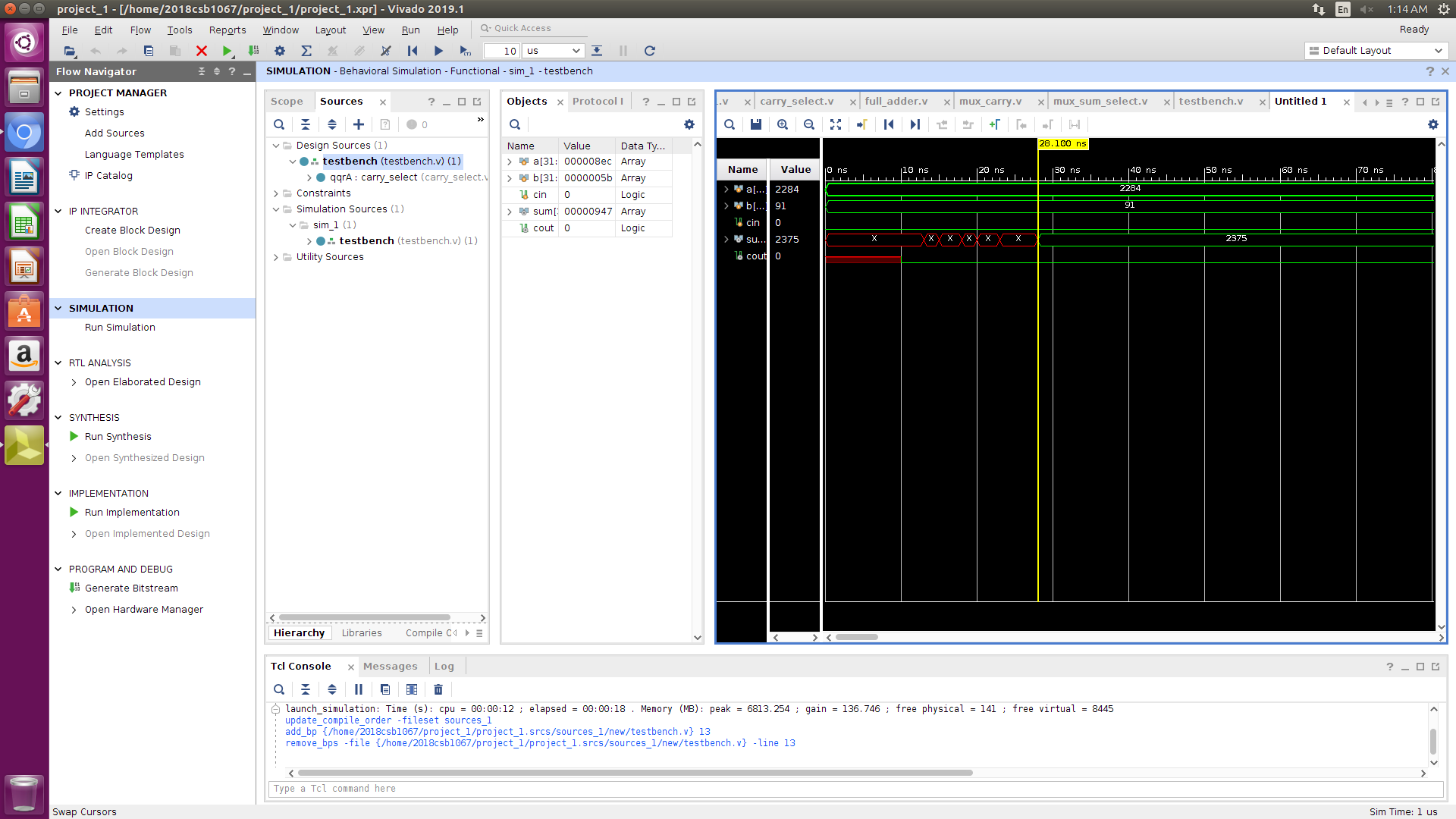
multiplexers . The architecture of CSlA is illustrated in fig.



**Delay:**

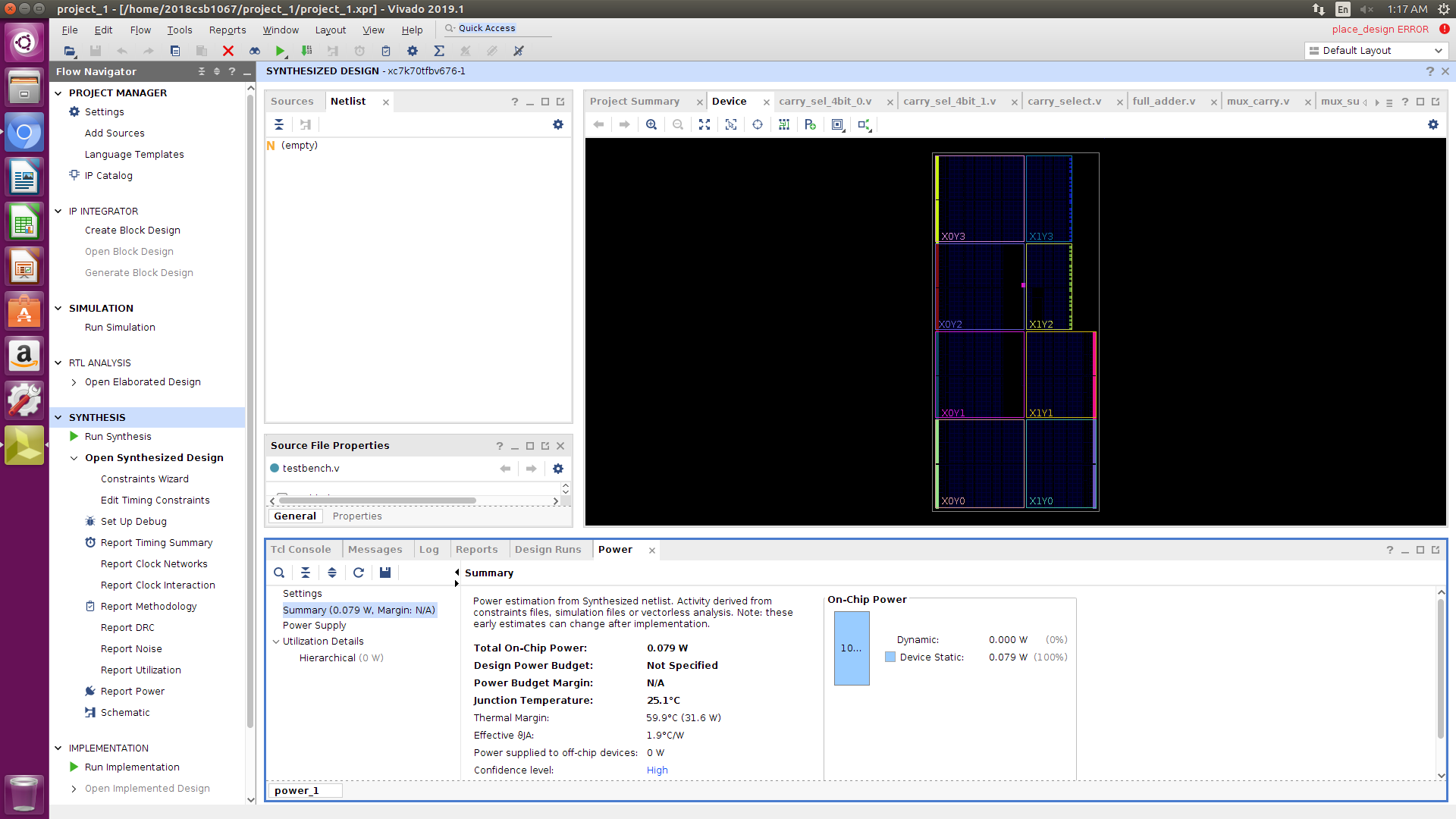
The delay and output graph of Carry select adder is attached below for a given set of input.

The use of muxes in carry select adder increases its complexity as compared to CLA.



# **Power Analysis:**

# The power consumed of the given adder is as estimated as follows:



CARRY SKIP ADDER:

As the name indicates, Carry Skip Adder (CSkA) uses skip logic

in the propagation of carry . It is designed to speed up the

addition operation by adding a propagation of carry bit around a

portion of entire adder.

The carry-in bit designated as Ci. The output of RCA (the last

stage) is Ci+4. The Carry Skip circuitry consists of two logic gates.

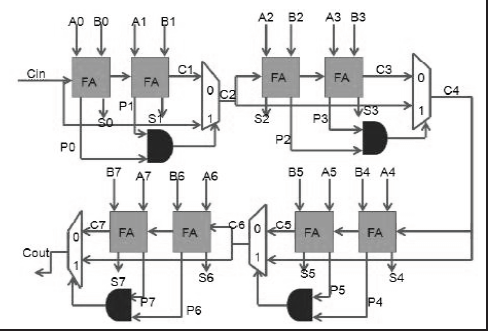
AND gate accepts the carry-in bit and compares it with the group

of propagated signals given below.

P([i,i+3]) = P(i+3)\*P(i+2)\*P(i+1)\*P(i)

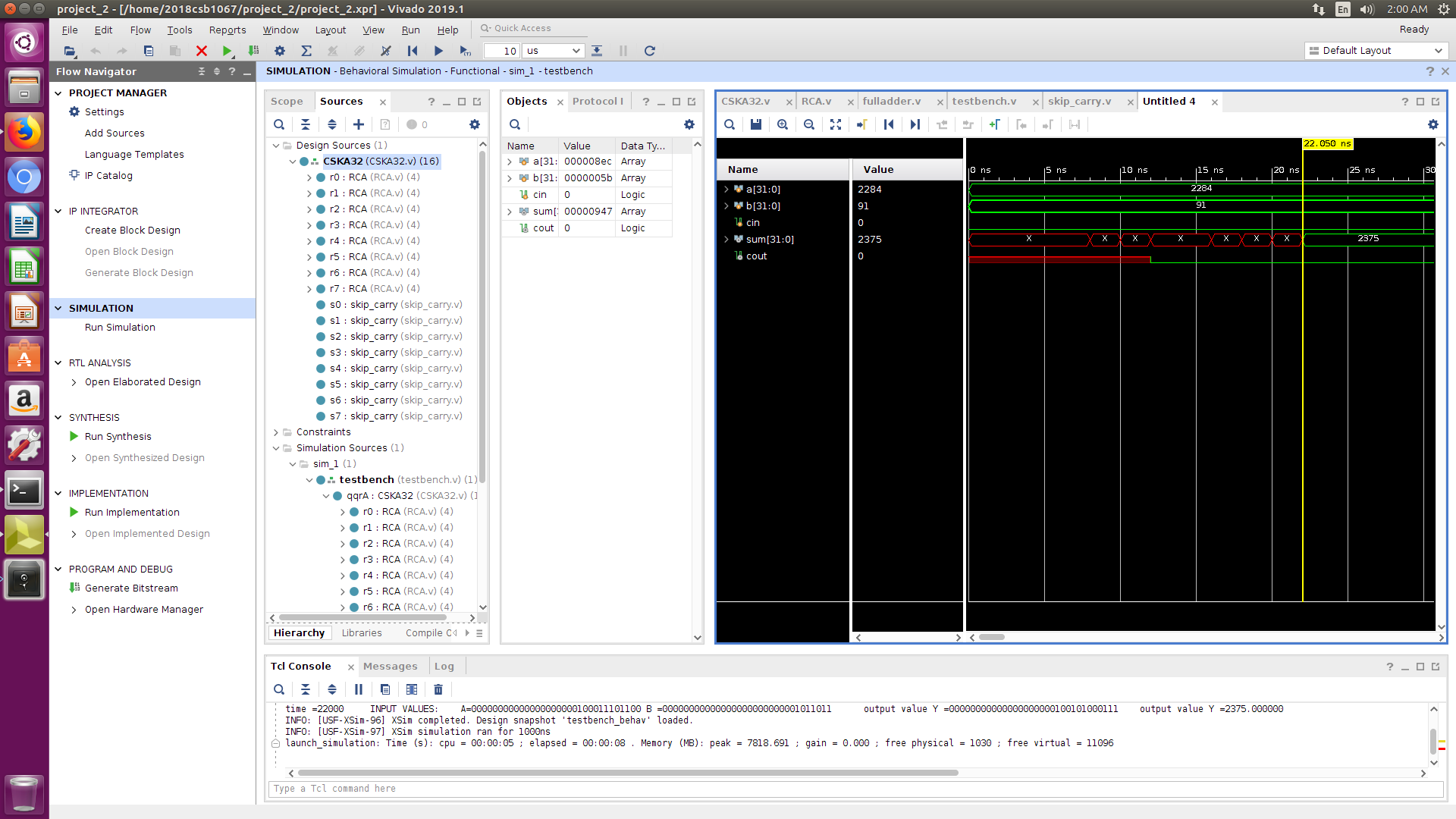
Carry = C(i+4) + P([i, i+3])\* C(i)

Block Diagram is shown for a given set of inputs a and b.



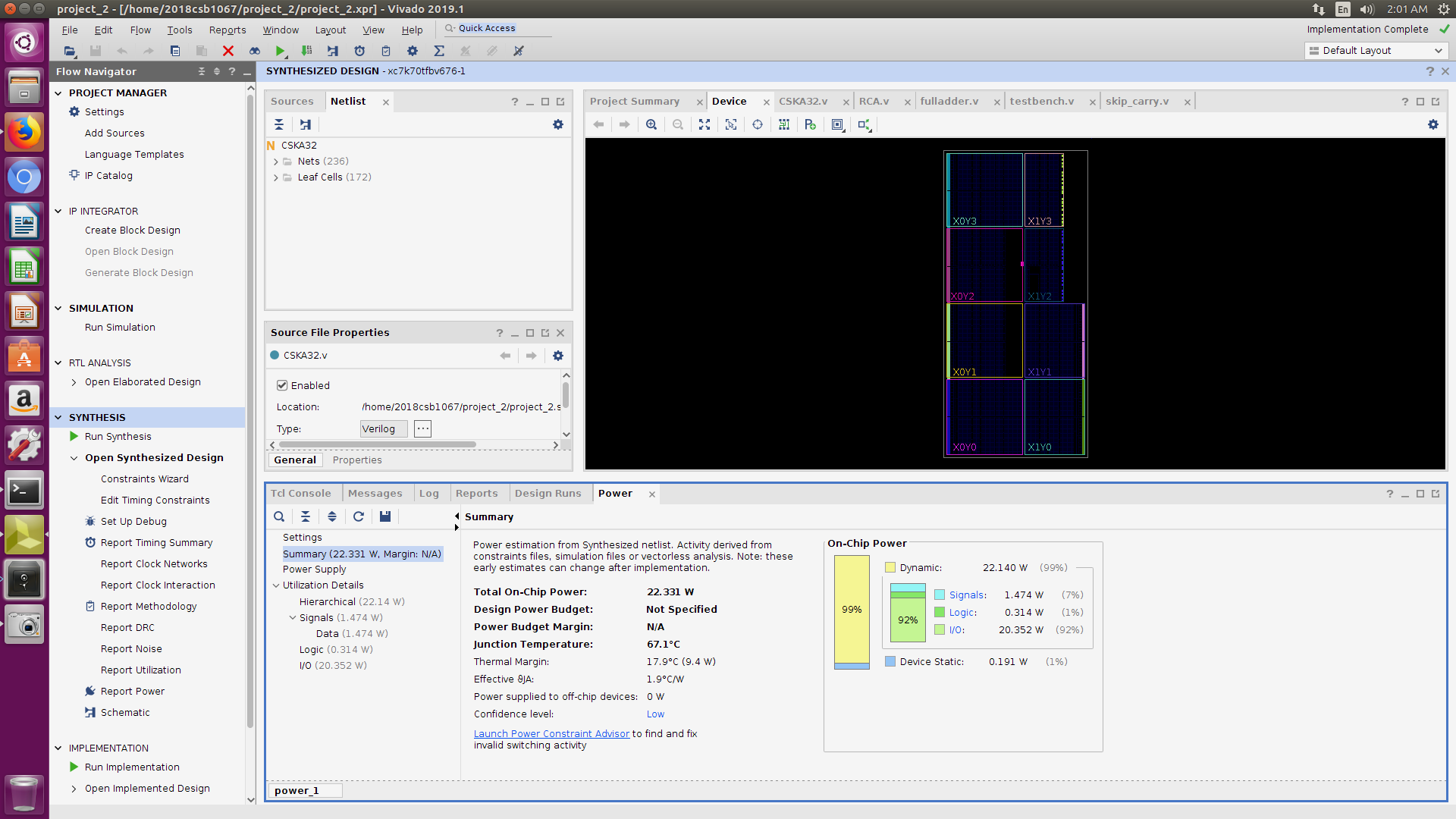
**Delay:**

The delay and output graph of Carry skip adder is attached below for a given set of input.



**POWER ANALYSIS:**

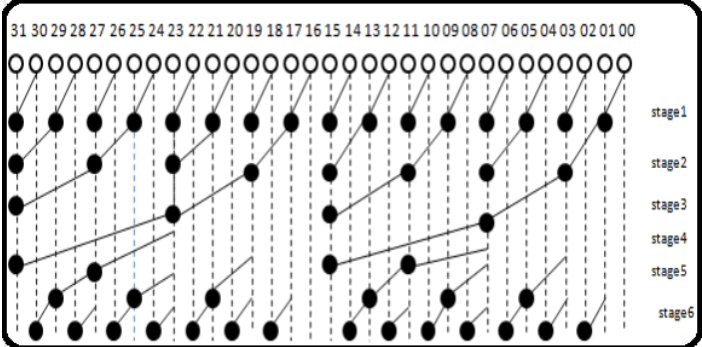
The power consumed of the given adder is as estimated as follows:



**BRENT KUNG ADDER**

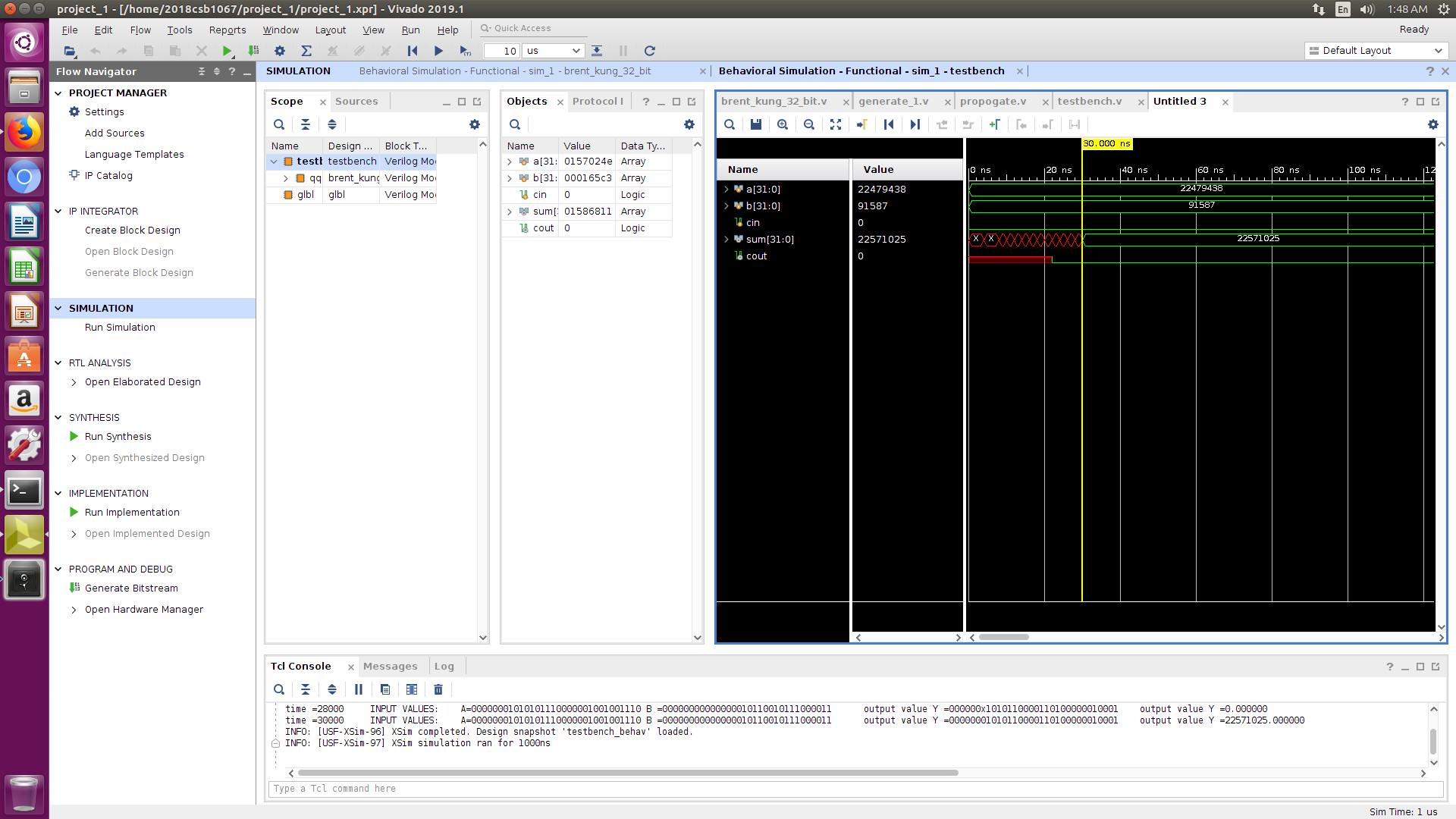
A Brent–Kung adder is a parallel adder made in a regular layout with an aim of minimizing the chip area and ease manufacturing. The addition of n-bit number can be performed in time O(log(n)),

thus making it a good-choice adder with constraints on area and maximizing the performance. Its symmetry and regular build structure reduces costs of production effectively and enable it to be used in pipeline architectures. In parallel adders the critical path is decided by computation of the carry from [least significant bit](https://en.wikipedia.org/wiki/Least_significant_bit) (LSB) adder to the [most significant bit](https://en.wikipedia.org/wiki/Most_significant_bit) (MSB) adder, therefore efforts are in reducing the critical path for the carry to reach the MSB.



**Delay:**

The delay and output graph of BRENT KUNG adder is attached below for a given set of input.



**POWER ANALYSIS**:

The power consumed of the given adder is as estimated as follows:

